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interconnection comprises solid state connection of the interconnection bumps with a complementary arrangement of interconnect pads on the first surface of the substrate.

REMARKS

The specification and drawings have been proofread, and are amended herein to correct obvious errors of a typographical or editorial nature. Claim 5 is deleted, without disclaimer or prejudice to Applicants' right to prosecute claims to the subject matter thereof by way of one or more continuing applications. Claim 1 is amended to incorporate certain recitations of claims 5 and 2; and claim 2 is amended for improved clarity. No new matter is introduced by any of the amendments, and entry thereof is requested. Claims 1-4 and 6-11 are in the application. Reconsideration of the application, as amended, is requested.

The specific points raised by the Examiner will now be addressed, beginning with the rejections under 35 U.S.C. §102.

Rejections under 35 U.S.C. § 102(e) and 35 U.S.C. § 102(b)

Claims 1-4, 6-9 and 11 were rejected under 35 U.S.C. § 102(e) as being anticipated by Rolda, Jr., US 2002/0030261 A1 ("Rolda"); and claims 1-4 and 6-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Inaba *et al.* U.S. 6,166,443 ("Inaba").

Claim 1 is amended herein to recite that the flip chip interconnection, that is, the connection of the interconnect bumps affixed to the chip with the pads on the substrate, is a solid state connection. Neither Rolda nor Inaba teaches or suggests solid state interconnect and, accordingly, the rejections for anticipation can be withdrawn.

Rejection under 35 U.S.C. § 103(a)

The Examiner apparently viewed at least some of the claims as being product-by-process claims. Claim 5 was rejected under 35 U.S.C. § 103(a) for obviousness over either Rolda or Inaba, the Examiner citing MPEP § 2113 as grounds for rejection under Section 103.

Claim 5 has been deleted, and claim 1 has been amended to recite that the flip chip interconnection is a solid state connection of interconnect bumps affixed to the die with interconnect pads on the first surface of the substrate.

As for MPEP 2113, the claims have been amended to remove process recitations (*e.g.*, recitations that connection "is made by"), and the claims as amended are accordingly clearly directed to the structure. The meaning of "solid state" connection is clearly defined in Applicants' specification (*See, e.g.*, paragraph [0026] at page 4, lines 31-34). Solid state flip chip interconnection according to the invention has significant advantages; particularly, chip scale packages according to the invention can have significantly finer pitch and significantly thinner gap between the die surface and the substrate than interconnects formed by melted solder bond (*See, e.g.*, Applicants' specification paragraph [0026] at page 4, lines 34-36; paragraph [0027] at page 5, lines 1-12).

Solid state flip chip interconnect is neither taught nor suggested by Rolda or Inaba, nor by any combination of them and, accordingly, the rejections for obviousness can be withdrawn.

In view of the foregoing, it is believed that all the claims in the application are in condition for allowance, and action to that effect is requested.

This response is being filed within the second month following the shortened statutory period set by the Examiner and, accordingly, it is accompanied by a petition for two months' extension of time and a fee or fee authorization therefor. In the unlikely event that the petition or fee may become separated from this paper, or if the Examiner determines that a further extension of time is required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge the fee to Deposit Account 50-0869 (Order No. CPAC 1010-2).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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